IFW

CERTIFICATE OF DELIVERY BY HAND
I hereby certify that this correspondence is being hand delivered to the USPTO, Customer Service Window, Randolph Building, 401 Dulany Street, Alexandria Virginia 22314 by the person whose name appears at the bottom of page 7 of this document

Signed: Deborah Cameron
Deborah Cameron

OIPE IAP68 NOV 2 8 2005 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Subir Ghosh and Hsu-Tien Tung**	Attorney Docket No.: **OPTI 3140-6**
Application No.: **10/619,798**	Examiner: **ELLIS, Kevin L.**
Filed: **July 15, 2003**	Group: **2188**
Title: **PREDICTIVE SNOOPING OF CACHE MEMORY FOR MASTER-INITIATED ACCESSES**	Confirmation No.: **Not Known**
	Customer No. **22470**

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

United States Patent and Trademark Office
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

It is requested that the information identified in this statement be considered by the Examiner and made of record in the above-identified application. This statement is not intended to represent that a search has been made or that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 C.F.R. 1.56.

Since this is a continuation, divisional or continuation-in-part application, it is understood that the Examiner will consider all information which was considered by the Office in a parent application. MPEP 609.

Enclosed with this statement is a Form PTO/SB/08A. The Examiner is requested to initial the form and return it to the undersigned in accordance with M.P.E.P. 609.

This statement should be considered under 37 C.F.R. 1.97**(b)** because it is being filed before the mailing date of the first Office Action after the filing of a Request for Continued Examination under 37 C.F.R. 1.114.

Fee Authorization. The Commissioner is hereby authorized to charge underpayment of any additional fees or credit any overpayment associated with this communication to Deposit Account No. 50-0869 (OPTI 3140-6). A duplicate copy of this authorization is enclosed.

Respectfully submitted,

Haynes Beffel & Wolfeld LLP

Date: November 23, 2005 By: _____
Warren S. Wolfeld, Reg. No. 31,454

Haynes Beffel & Wolfeld LLP
P.O. Box 366; 751 Kelly Street
Half Moon Bay, CA 94019
Ph. (650) 712-0340
Fax (650) 712-0263

CERTIFICATE OF DELIVERY BY HAND

I hereby certify that this correspondence is being hand delivered to the USPTO, Customer Service Window, Randolph Building, 401 Dulany Street, Alexandria, Virginia 22314

By Annette Masiello Date: Nov. 28, 2005
Signature

Print Name: Annette Masiello

Please type a plus sign (+) inside this box → [+]

PTO/SB/08B (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U. S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

OIPE IAP68 NOV 28 2005 PATENT & TRADEMARK OFFICE

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 3

Complete if Known	
Application Number	10/619,798
Filing Date	15 July 2003
First Named Inventor	Subir Ghosh
Group Art Unit	2188
Examiner Name	ELLIS, Kevin L.
Attorney Docket Number	OPTI 3140-6

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	C1	MOTOROLA INC., "PowerPC 601 RISC Microprocessor Technical Summary", Freescale Semiconductor, Inc., 1993	
	C2	NORMAN P. JOUPPI, "Improving Direct-Mapped Cache Performance by the Addition of a Small Fully-Associative Cache and Prefetch Buffers, 18 Computer Architecture News 364-373, 1990	
	C3	NORMAL P. JOUPPI, "Reducing Compulsory and Capacity Misses", WRL Technical Note TN-53, August 1990	
	C4	FREDRIK DAHLGREN ET AL., "Sequential Hardware Prefetching in Shared-Memory Multiprocessors", 6 IEEE Transactions on Parallel and Distributed Systems 733-746 , 1995	
	C5	DEAN M. TULLSEN, SUSAN J. EGGERS, "Limitation of Cache Prefetching on a Bus-Based Multiprocessor", Proceedings of the 20th Annual International Symposium on Computer Architecture at 278-88, 1993	
	C6	WILLIAM Y. CHEN ET AL., "Data Access Microarchitectures for Superscalar Processors with Compiler-Assisted Data Prefetching", Proceedings of the 24th Annual International Symposium on Microarchitecture at 69-73, 1991	
	C7	ALAN JAY SMITH, "Cache Memories", 14 ACM Computing Surveys 473-530, 1982	
	C8	JEAN-LOUP BAER & TIEN-FU CHEN, "An Effective On-Chip Preloading Scheme to Reduce Data Access Penalty", In Proceedings of Supercomputing '91 at 176-86, 1991	
	C9	TIEN-FU CHEN & JEAN-LOUP BAER, "Effective Hardware-Based Data Prefetching for High Performance Processors, 44 IEEE Transactions on Computer 609-623, May 1995	
	C10	TIEN-FU CHEN & JEAN-LOUP BAER, "A Performance Study of Software and Hardware Prefetching", 22 Computer Architecture News 223-232, 1994	
	C11	TIEN-FU CHEN & JEAN-LOUP BAER, "Reducing Memory Latency via Non-blocking and Prefetching Caches", Fifth International Conference on Architectural Support for Programming Languages and Operating Systems at 51-61, 1992	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Unique citation designation number. [2] Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U. S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Please type a plus sign (+) inside this box → [+]

PTO/SB/08B (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U. S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 2 of 3

Complete if Known	
Application Number	10/619,798
Filing Date	15 July 2003
First Named Inventor	Subir Ghosh
Group Art Unit	2188
Examiner Name	ELLIS, Kevin L.
Attorney Docket Number	OPTI 3140-6

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	C12	LUCIEN CENSIER & PAUL FEAUTRIER, "A New Solution to Coherence Problems in Multicache Systems", 27 IEEE Transactions on Computers 1112-1118, 1978	
	C13	MICHEL DUBOIS ET AL., "Memory Access Buffering in Multiprocessors", 14 Computer Architecture News 434-442, 1986	
	C14	JOHN W.C. FU & JANAK H. PATEL, "Data Prefetching in Multiprocessor Vector Cache Memories", Proceedings of the 18th Annual International Symposium on Computer Architecture at 54-63, 1991	
	C15	JOHN W.C. FU & JANAK H. PATEL, "Stride Directed Prefetching in Scalar Processors", Proceedings of the 25th Annual International Symposium on Microarchitecture at 102-10, 1992	
	C16	EDWARD H. GORNISH ET AL., "Compiler-Directed Data Prefetching in Multiprocessors with Memory Hierarchies", Proceedings of the 1990 International Conference on Supercomputing at 354-368, 1990	
	C17	ALEXANDER C. KLAIBER & HENRY M. LEVY, "An Architecture for Software-Controlled Data Prefetching", Proceedings of the 18th Annual International Symposium on Computer Architecture at 43-53, 1991	
	C18	DAVID KROFT, "Lockup-Free Instruction Fetch-Prefetch Cache Organization", Proceedings of the 8th Annual International Symposium on Computer Architecture at 81-5, 1981	
	C19	ROLAND L. LEE, "The Effectiveness of Caches and Data Prefetch Buffers in Large-Scale Shared Memory Multiprocessors", (May 1987) (Ph.D. thesis, University of Illinois at Urbana-Champaign)	
	C20	ROLAND L. LEE ET AL., "Data Prefetching in Shared Memory Multiprocessors, Proceedings of the 1987 International Conference on Parallel Processing at 28-31, 1987	
	C21	TODD C. MOWRY ET AL., "Design and Evaluation of a Compiler Algorithm for Prefetching", Fifth International Conference on Architectural Support for Programming Languages and Operating Systems at 62-73, 1992	
	C22	ALLAN K. PORTERFIELD, "Software Methods for Improvement of Cache Performance on Supercomputer Applications (May 1989) (Ph.D. thesis, Rice University)	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Unique citation designation number. [2] Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U. S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Please type a plus sign (+) inside this box → [+]

PTO/SB/08B (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U. S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 3 of 3

Complete if Known	
Application Number	10/619,798
Filing Date	15 July 2003
First Named Inventor	Subir Ghosh
Group Art Unit	2188
Examiner Name	ELLIS, Kevin L.
Attorney Docket Number	OPTI 3140-6

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	C23	TIEN-FU CHEN, "Data Prefetching for High-Performance Processors (July 1993) (Ph.D. Thesis, University of Washington)	
	C24		

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Unique citation designation number. [2] Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U. S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.